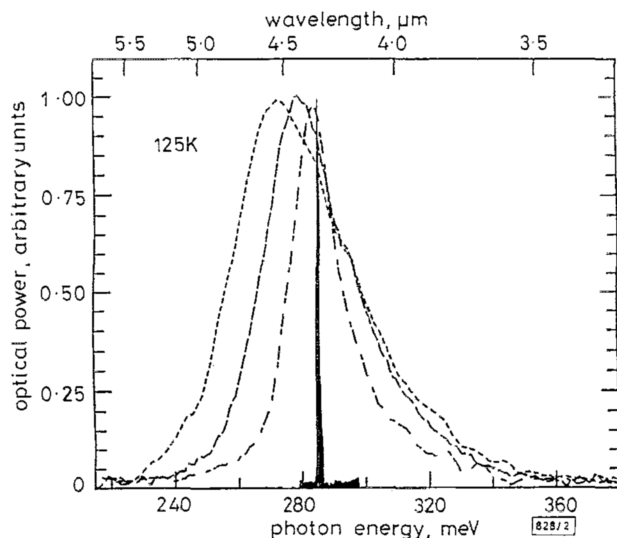

Fig. 2 *Normalised emission spectrum of quantum cascade laser below and above threshold for four different drive currents*

The light is polarised normal to the layers

show, respectively, the low and high resolution spectrum of the laser at 125K, providing direct evidence of laser action from the strong line narrowing and clearly illustrating the longitudinal mode structure. The separation of these modes is in good agreement with the calculated value ($1/2nL = 0.55\,cm^{-1}$). The width of dominant mode is ~$0.3\,cm^{-1}$, limited by heating and mode hopping during the pulse.

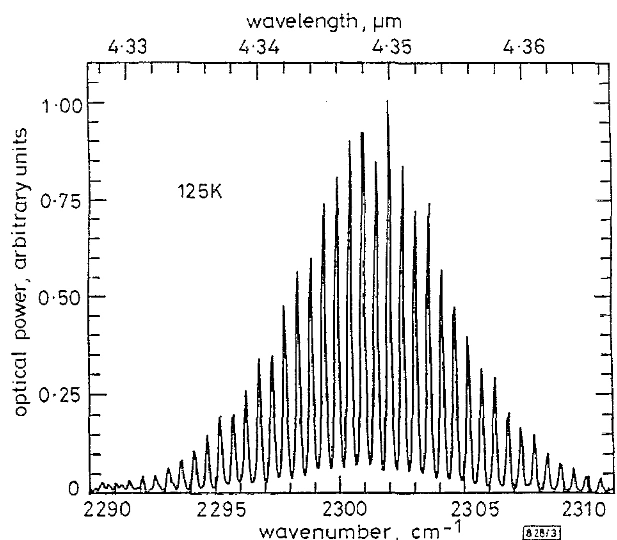

Fig. 3 *High resolution emission spectrum showing the longitudinal mode structure*

The drive current is 6.5mA

From the expression of the threshold current density, $J_{th} = (\alpha_M + \alpha_i)/g\Gamma$, where α_M is the mirror loss (= $4.8\,cm^{-1}$), α_i the internal loss (estimated $\simeq 9\,cm^{-1}$) and g is the peak gain coefficient (estimated $\simeq 9\,cm^{-1}$ per kA/cm^2 from spontaneous emission measurements at 10K using the ratio of the Einstein coefficients), we obtain $J_{th} = 3.3\,kA/cm^2$ at 10K, in reasonable agreement with the measured value. From the measured slope efficiency (~0.1W/A in the 10–100K range), which is proportional to the number of periods, and the estimate of the collection efficiency and losses, we estimate an internal quantum efficiency $\eta_i = 0.2$. We believe that η_i is limited by intervalley scattering, due to the small energy difference between state 3 and the L valleys in GaInAs, and by spatial hole burning.

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Thermal comparison of long-wavelength vertical-cavity surface-emitting laser diodes

J. Piprek and S.J.B. Yoo

Indexing terms: Vertical cavity surface emitting lasers, Heat transfer

Heat flow finite element analysis is applied to basic device concepts, including planar structures with InGaAsP/InP or AlAs/GaAs substrate side mirrors (mounted top-up or top-down) and etched-well lasers with Si/SiO_2 dielectric mirrors. In several cases, the calculated thermal resistance values are higher than with short-wavelength devices, but wafer-fused structures on GaAs substrate show clear thermal advantages.

Introduction: Long-wavelength (1.3–1.55µm) vertical-cavity surface-emitting lasers (LW-VCSELs) are a promising new generation of light sources for long-distance optical communication systems. Owing to several advantages in testing, optical coupling, singlemode operation and modulation, they have the potential to replace conventional edge-emitting laser diodes in many existing applications. In contrast to the rapid development of short-wavelength (0.8–1.0µm) VCSELs within the last few years, near room temperature (14°C) CW operation of an electrically pumped 1.3µm device has been achieved only recently [1]. This contrast is mainly attributed to the InGaAsP material system with larger Auger nonradiative recombination, higher intervalence band absorption, lower thermal conductivity, and smaller refractive index variation than in the short-wavelength (SW) AlGaAs system. Thus, different concepts of LW-VCSELs are currently competing, featuring different materials for the substrate side (bottom) distributed Bragg reflector (DBR): InGaAsP/InP [2, 3], AlAs/GaAs [4, 5], or dielectric materials, e.g. SiO_2/Si [1, 6]. The top DBR is commonly an SiO_2/Si [3, 5, 6], Al_2O_3/Si [2] or Si_3N_4/Si [4] dielectric mirror, whereas an MgO/Si DBR with higher bulk material thermal conductivity κ was used to achieve the 14°C CW performance of the top-down mounted device in [1]. Laser heating is a key problem in all of these devices, i.e. minimising the thermal resistance R_{th} between the active region and the heatsink is a major issue for successful LW-VCSEL operation. Thermal modelling has been applied to two of these structures. Shimizu *et al.* [7] investigated an etched-well laser with top and bottom dielectric mirrors (Si_3N_4/Si) by the finite difference method. The analytical approach of Osiński and Nakwaski [8] to top-up mounted lasers with semiconductor bottom mirrors replaces the multilayer laser structure by one effective material and neglects heat spreading layers above the heat source. This Letter compares the thermal resistances of various LW-VCSEL devices by quasi-three-dimensional finite element analysis including top-up or top-down mounting and lateral embedding of the active region in different regrowth materials (polyimide and semi-insulating InP, respectively). The central part of the simulated 1.55µm VCSELs (see [3, 5, 6]) is displayed in Fig. 1 with five pairs of SiO_2/α-Si forming the top dielectric mirror, a 270 nm thick Au contact, and the 162nm thick InGaAsP active

region sandwiched between a 900nm top spacer and 650nm bottom spacer, connected to different choices of bottom mirror. Substrate thickness and device radius are 100μm; the diameter of the active region is 10μm.

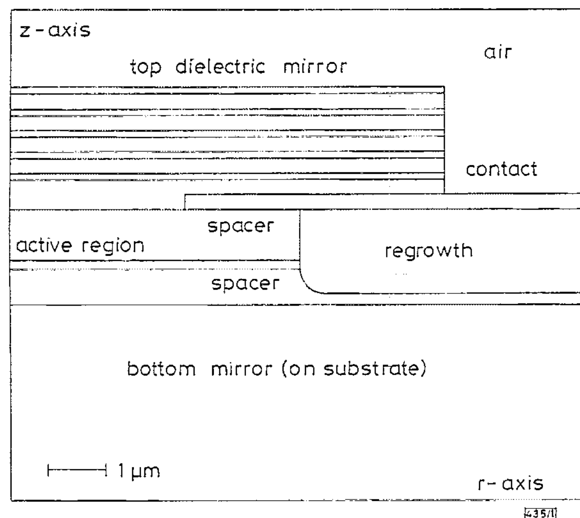

Fig. 1 *Diagram of top central LW-VCSEL section in cylindrical coordinates as assumed in calculations (top-mounted case)*

Thermal model: The cylinder symmetrical temperature distribution $T(r,z)$ within the VCSEL is obtained by solving the thermal conduction equation

$$-\left[\frac{\partial}{\partial r}\kappa_r\frac{\partial T}{\partial r}+\frac{1}{r}\kappa_r\frac{\partial T}{\partial r}+\frac{\partial}{\partial z}\kappa_z\frac{\partial T}{\partial z}\right]=\frac{\partial P}{\partial V}(r,z) \qquad (1)$$

using multi-purpose finite element software [9]. In eqn. 1, $\partial P/\partial V$ gives the heat power density distribution, and $\kappa(r,z)$ denotes the thermal conductivity of bulk material in the vertical (κ_z) or radial (κ_r) direction. Anisotropic behaviour ($\kappa_z \neq \kappa_r$) occurs in multilayer materials, as in semiconductor DBR stacks, which involve about 20 to 40 pairs of thin layers (thickness d_1 and d_2, respectively) with different bulk thermal conductivities (κ_1 and κ_2, respectively). Employing the simple model of serial and parallel thermal resistances, respectively, the two components of the DBR thermal conductivity are calculated as (see eqns. 2 and 3 in [8])

$$\kappa_r=\frac{d_1\kappa_1+d_2\kappa_2}{d_1+d_2} \text{ and } \kappa_z=\frac{d_1+d_2}{d_1/\kappa_1+d_2/\kappa_2} \qquad (2)$$

Thus, the heat conduction within multilayer DBRs is stronger in the radial direction than in the vertical direction (anisotropy due to phonon mean free path restrictions by the layer boundaries [10] is assumed insignificant in our case, where DBR sheets are thicker than 100nm). The thermal conductivity depends on the temperature, but in this analysis the total heat power is kept low enough to neglect the dependency $R_{th}(T)$. Moreover, for thermal comparison of different laser structures, the heat power density $\partial P/\partial V(r,z)$ is simplified to be uniform and restricted to the active region. Therefore, the thermal resistance can be calculated as a characteristic parameter of the laser structure by dividing the maximum temperature rise in the active region (relative to the heatsink) by the total heat power

$$R_{th}=\Delta T_{max}/P_{heat} \qquad (3)$$

Modelling results: For comparison, the finite element analysis is first applied to a typical short-wavelength (0.98μm) gain-guided VCSEL as analysed in [11] with the 76nm thick InGaAs active region sandwiched between 355nm thick stepped-index AlGaAs spacer layers and AlAs/GaAs DBRs on GaAs substrate. The resulting thermal resistance is 870K/W in the top-emitting case and 550K/W with the laser diode mounted top-down on the heatsink (active region radius: 5μm, device radius and substrate thickness: 100μm). As usual, top-down mounting lowers the thermal resistance because the heat source is closer to the heatsink. Here and in the following, the top-down mounting In solder thickness is 3 μm (κ = 0.87$Wcm^{-1}K^{-1}$). Table 1 summarises all results of this R_{th} comparison. Adapting the SW device to the structure in Fig. 1, i.e. replacing the planar top AlAs/GaAs DBR by the SiO_2/α-Si DBR and Au contact, the R_{th} values increase to 1200K/W (top-up) and 910K/W (top-down). Obviously, forming the top DBR out of SiO_2 and α-Si layers (κ = 0.014 and 0.026$Wcm^{-1}K^{-1}$, respectively) restricts not only the thermal flux for top-down mounting. The missing radial heat conduction in the top AlAs/GaAs DBR (κ_r = 0.69$Wcm^{-1}K^{-1}$, κ_z = 0.61$Wcm^{-1}K^{-1}$) also limits the heat flow with substrate side heatsink.

Table 1: Calculated thremal resistances R_{th} [K/W] of VCSEL versions described in the text

Laser on heatsink mounting:	Top-up	Top-down
Short-wavelength VCSEL:		
AlAs/GaAs-DBR, planar	870	550
n-AlAs/GaAs-DBR, adapted	1200	910
Long-wavelength VCSEL:		
n-AlAs/GaAs-DBR on GaAs	870 (1060)	610 (830)
n-InGaAsP/InP-DBR on InP	1450 (2020)	880 (1190)
SiO_2/Si-DBRs, etched well	-	1090 (1620)
Values in parentheses: with polyimide regrowth instead of InP; prefix n denotes n-doped bottom mirror		

The use of an AlAs/GaAs n-DBR (n-doped) on GaAs substrate within long-wavelength wafer-fused InP VCSEL structures [4, 5] requires a higher thickness of single DBR layer than in the SW version and increases the thermal resistance of the bottom DBR. However, the heat source is now embedded in InP, having a higher thermal conductivity (0.68$Wcm^{-1}K^{-1}$) than the SW stepped-index $Al_xGa_{1-x}As$ spacer (κ = 0.44–0.06$Wcm^{-1}K^{-1}$ for x = 0–0.5). Hence, the calculated R_{th} = 870K/W (top-up) is smaller than for the adapted SW-VCSEL, even with polyimide (κ = 0.0016$Wcm^{-1}K^{-1}$) regrowth, which strongly restricts the radial heat flux: R_{th} = 1060K/W. Mounting this LW-VCSEL top-down also results in lower values compared to the adapted SW-VCSEL: R_{th} = 610 K/W (with polyimide: 830K/W).

An alternative LW-VCSEL version replaces the AlAs/GaAs bottom part of the previous structure by a 42 pair InGaAsP/InP n-DBR on InP substrate [3]. Owing to the highly different thermal conductivities of the mirror materials, κ is now much lower in the vertical than in the radial direction (κ_z = 0.078$Wcm^{-1}K^{-1}$, κ_r = 0.35 $Wcm^{-1}K^{-1}$). Despite the higher thermal conductivity of the InP substrate, the total thermal resistance of the top-up mounted chip is 1450K/W, because the n-DBR acts as a much stronger heat barrier than in the former examples. This tendency is the opposite of the analytical result in [8], which predicts smaller R_{th} values in InGaAsP/InP VCSELs than in SW-VCSELs. With polyimide, R_{th} even rises to 2020 K/W. Better thermal behaviour can be achieved by top-down mounting; in the present case the thermal resistance drops to 880 K/W (with polyimide: 1190K/), which is still higher than with the AlAs/GaAs LW-VCSEL due to weaker heat spreading within the n-DBR.

The often preferred top-down mounted LW-VCSEL structure with dielectric mirrors on both sides shows a bottom DBR which is placed within a well etched into the InP substrate. For comparison, the former semiconductor bottom DBR is replaced by five pairs of SiO_2/α-Si with 60μm diameter within the InP well (see [6]). The bottom DBR thermal conductivity is even lower than in the examples above, and the thermal resistances of 1090K/W (with InP) and 1620K/W (with polyimide) are the highest top-down values of this comparison. Slightly higher numbers are calculated in [7], where a thicker spacer layer and a smaller device diameter (60μm) are assumed.

Conclusion: Comparing the calculated thermal resistances of basic LW-VCSEL versions, wafer-fused structures with AlAs/GaAs bottom DBR on GaAs substrate show clear advantages with a minimum value of R_{th} = 610K/W (top-down, InP regrowth). Besides a high thermal conductivity of the bottom DBR, a broad heat spreading within the spacer layers is found to be essential for obtaining low thermal resistances.

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New mounting technique for two-terminal millimetre-wave devices

T. Bauer and J. Freyer

Indexing terms: Packaging, Solid-state microwave devices

A new mounting technique for two-terminal devices is presented which minimises parasitic elements and improves thermal heat resistance. Monolithic fabrication of the structure leads to high reproducibility. First experimental results for power generation at W-band frequencies with GaAs Impatt diodes are reported.

Introduction: Two-terminal devices are used in a variety of millimetre-wave applications. To ensure optimum device performance, impedance matching of the active device and resonator structure is an important design consideration. The parasitic elements, caused by the mounting, transform the active device impedance and normally lead to a reduction of power and efficiency as well as maximum frequency.

The technology of employing quartz stand-offs or rings together with gold-ribbons is in widespread use. For this technique, the parasitic elements depend to a high degree on the manually defined geometry and therefore considerable variations are possible, especially when high frequencies are desired. Additionally, the high cost of manually encapsulating one single element is enormous. Planar technology has proven to be an effective means of overcoming these difficulties leading to monolithically integrated oscillators [1, 2]. However, as a result of the relatively high losses and poor heat transfer, the application of planar technology is restricted to frequencies below ~100GHz.

Tschernitz and Freyer proposed a millimetre-wave module using semi-insulating GaAs material as stand-off elements [3], which allows precise control of the parasitic elements and particularly a minimisation of the parasitic inductance. Reduction of the parasitic capacitance, however, is limited by the remaining semi-insulating GaAs material with its comparatively large dielectric constant.

In this paper we present a new mounting technique, where semi-insulating GaAs material is totally omitted. Instead, a self-supporting structure of three active devices is proposed.

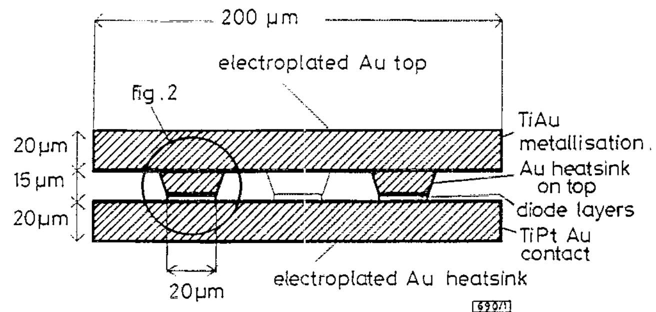

Fig. 1 *Schematic cross-section of mounting technique with three GaAs IMPATT diodes*

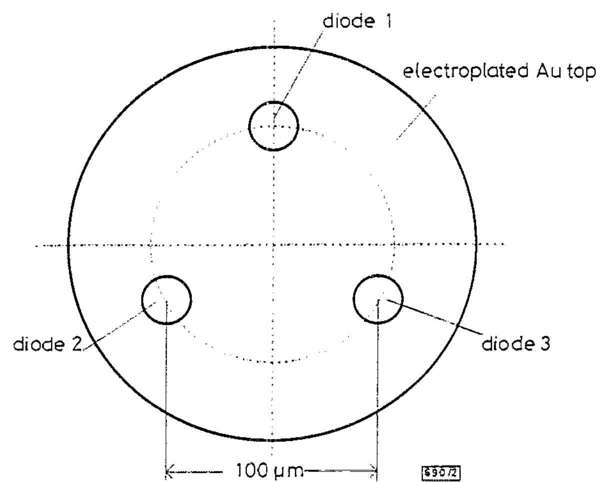

Fig. 2 *Top view showing position of diodes*

Mounting structure: The new mounting technique to be employed in waveguide cap resonators is based on an arrangement of three active devices with a gold heatsink on top, as depicted in Figs. 1 and 2. The active devices together with the top heatsink serve as a support for the resonator cap. This structure shows a variety of advantages compared to other encapsulation modes: Most important is the possibility of minimising the parasitic elements, allowing operation at elevated frequencies. The parasitic inductance is determined only by the size of the heatsink on top of the devices. Owing to the fact that no stand-off material is applied, the parasitic capacitance is as low as possible. As the whole structure is fabricated monolithically, all dimensions can be established precisely by photoresist technology and, therefore, a high reproducibility can be obtained.

Impedance matching between the active devices and the resonator structure is mainly determined by the diameter of the cap and its height above the bottom of the waveguide [4]. This height can be exactly controlled by the size of the heatsinks on top of the active devices. In a further improvement, a cap with a certain diameter for a desired frequency can be integrated to realise a pretuned resonant structure.

Moreover, the heat dissipation capability is increased. By splitting one large device area into several sections, i.e. by using several devices with smaller area, the thermal spreading resistance is reduced [5]. Here, for three devices the spreading resistance is reduced by a factor of $\sqrt{3}$. Furthermore, the gold heatsinks on top of the devices allow additional heat dissipation, which is impossible in conventional encapsulation with gold ribbons less than 1µm thick. This reduced thermal resistance is important for application at elevated frequencies, as most of the active millimetre-wave devices are thermally limited.