# Simulation and design of plasmonic directional couplers: application to interference-based all-optical gates

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***Abstract*—The paper is focused on the design of optical components based on plasmonic multi-slot directional couplers. In particular, the design of an all-optical gate is proposed, whose operation is based on the coupling between three plasmonic slots. The device input wavelength is 1550 nm, typical of long-haul telecommunication systems. The device footprint is as small as $11\times6\,\mu m^2$ and the contrast ratio as an AND gate is about 5.8 dB. The two well-known Finite-Difference Time-Domain (FDTD) and Finite-Difference Eigenmode (FDE) methods are used for the device simulation and optimization.**

## I. Introduction

All-optical gates and switches have been proposed both as an alternative to electro-optic components for optical routing/switching and as a building block for logical circuits overcoming fundamental limitations of electronic circuits [1]. All-optical gates typically require optical nonlinearities, see e.g. [2], but interference-based designs using linear materials have also been proposed, that are easier to fabricate [3], [4]. All-optical gates may exploit different device concepts, like the Mach-Zehnder interferometer [5], [6], the ring resonator [7] and, for interference-based gates, the Y-junction [3]. In this work, we present an interference-based all-optical gate exploiting plasmonic directional couplers. After preliminary studies on coupled plasmonic slot waveguides, the geometry is discussed and simulated with FDTD and FDE codes [8].

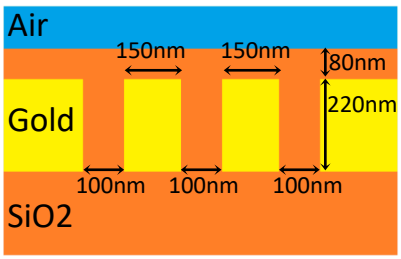


Fig. 1. Geometry of the three-slot directional coupler.

## II. The plasmonic directional coupler

The plasmonic slot consists of a dielectric layer ($SiO_2$ here) sandwiched between two metal layers (Au). If the three slots are close enough, the optical power is coupled between them. Fig. 1 shows the cross section of a directional coupler consisting of three coupled plasmonic slots. The width of each slot is 100 nm and the distance between slots is 150 nm. Also, the height of slot is designed to be 220 nm. The plasmonic effective refractive index $n_{eff}$ is computed for a single slot and for the three-slot structure through the FDE method. Fig. 2 compares the modal plasmonic refractive indexes with that of $SiO_2$. For a single slot, there is a single propagating mode, with effective refractive index larger than that of $SiO_2$. For the three-slots coupler, three propagating modes exist, corresponding to globally odd and even field distributions in the coupled slots. The splitting in the refractive indexes increases with slot coupling and, in general, the geometry can operate as a directional coupler. If the optical power enters one of the directional coupler slots, after propagating for a certain coupling length, power is coupled to the other slots.

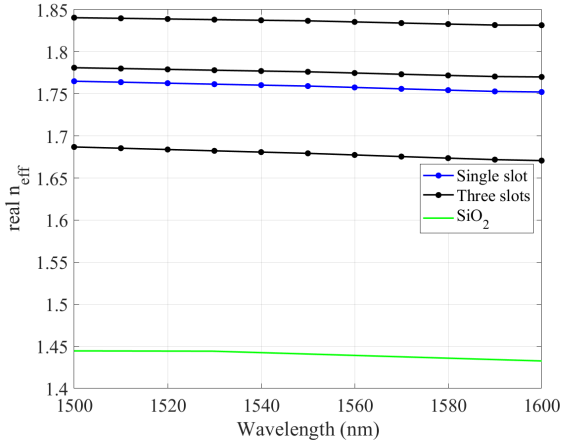


Fig. 2. Effective refractive index $n_{eff}$ of the single plasmonic slot and of the three-slot coupler versus wavelength.

## III. All-optical gate geometry and operation

All-optical interference-based gates (AND, OR, XOR) can be designed exploiting a three-slot directional coupler (instead

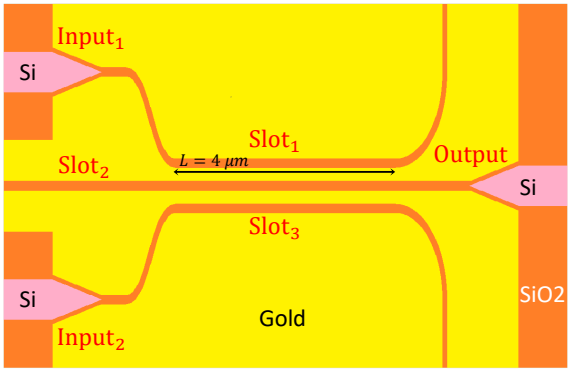


Fig. 3. Layout of the proposed AND plasmonic gate with photonic waveguide inputs and output.

of a Y-junction, as in [2]) as a power combiner. In this paper we concentrate on a gate that, with proper definition of the logical levels, operates as an AND gate. The gate geometry is shown in Fig. 3. The optical power from $\text{Input}_1$ and $\text{Input}_2$ are converted to $\text{Slot}_1$ and $\text{Slot}_3$, respectively, corresponding to the excitation of coupled modes. At the end of the coupler, the power in $\text{Slot}_2$ is converted into the output silicon photonic waveguide.

From a logical standpoint, four states can occur: in State 1, both inputs have zero optical power and the output power is zero. In the State 2 (State 3), the optical power only enters $\text{Input}_1$ ($\text{Input}_2$) and the output/input power ratio is 0.18. In State 4 the two input powers are equal and the output/input power ratio (where the input power is the one in each of the inputs) is 0.70. If output powers below 0.5 are considered as a logical 0, the geometry operates as an AND gate according to the truth tabel in Table I. Fig. 4 shows the absolute value of electric field for State 2 and 4; the output power ratio between State 4 and State 2 (State 3) is about 5.8 dB. The aforementioned values were obtained by optimizing the coupler length $L$ that affects the output/input power ratio in all logical states, as shown in Fig. 5; the contrast ratio between State 4 and State 2 (State 3) weakly depends on $L$, while, for $L \approx 4\,\mu$m (the selected design value), the optical insertion loss is minimum.

TABLE I
TRUTH TABLE OF AND GATE

| $\text{Input}_1$ | $\text{Input}_2$ | Output | Power Value |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0.18 |
| 0 | 1 | 0 | 0.18 |
| 1 | 1 | 1 | 0.70 |

## IV. Conclusions

In this simulation study, a multi-slot plasmonic directional coupler is proposed with application to the design of an AND all-optical gate gate. The gate size is about $11\times6\,\mu\text{m}^2$, making it suitable for integration and also, from a material standpoint, directly compatible with CMOS platforms.

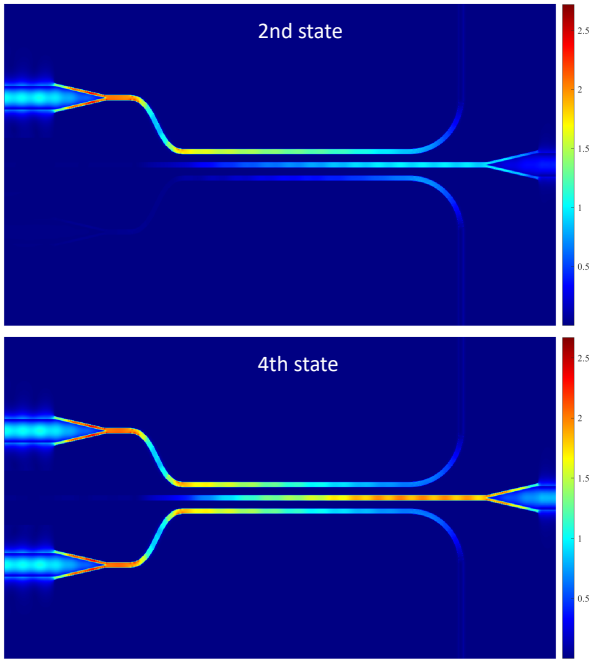


Fig. 4. The electric field for State 2 (above) and State 4 (below).

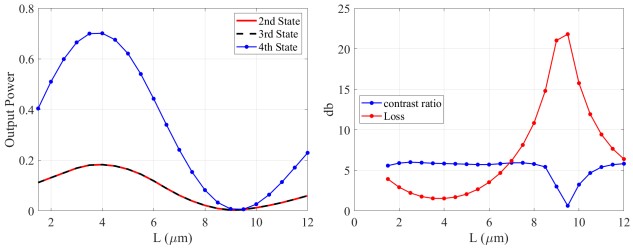


Fig. 5. Left: output power versus the directional coupler length $L$. Right: contrast ratio and losses versus $L$.

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