

Heterogeneous III-V/Si Photonic Integration: Configuration and Optical Coupling

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Abstract- This paper presents the overview of heterogeneous III-V/Si photonic integration configuration as a platform technology. The efficient adiabatic optical coupling between the active III-V/Si ridge waveguide and thin silicon-on-insulator (SOI) passive nanophotonic waveguide section is addressed.

Index Terms- photonic integration, optical coupling, heterogeneous III-V/Si

I. INTRODUCTION

Photonic integration based on from-wafer-to-chip manufacturing has been pursued over decades and the development of photonic integration has progressed from device-on-chip to system-on-chip, which is motivated to reduce the packaging cost of individual devices, and provide a high-performance/lightweight solution for practical applications in information-communication technologies, sensing and instrumentation etc. The challenge in realization of system-on-chip is the diversity of devices and materials required for the respective active and passive functionalities.

Among all the materials used in the integrated photonics, III-V compound semiconductor is an excellent substrate material for optoelectronics. Although it can be used for passive devices integration through regrowth or band-gap engineering, it has a small wafer-size and medium device size which are not favorable in cost and integration density. Silicon-on-insulator has the complementary advantages including high-density integration capability, large-scale wafer size and compatibility with existing silicon electronics manufacturing, but it is not an efficient material for active functionalities like light emission and amplification.

Heterogeneous III-V/Si photonic integration is a “new” platform as shown in Fig.1 which brings the III-V semiconductor epitaxial layers to silicon substrate (typically through wafer-bonding) so that we can fabricate the active and passive devices on the same substrate. It utilizes III-V compound semiconductors for active functionalities and silicon for the passive functionalities so that we can build a fully-integrated system-on-chip for various applications. Using heterogeneous III-V/Si integration as a platform technology requires 1) an efficient light confinement in III-V active region for light amplification; 2) a compact optical vertical optical interconnect access for effective adiabatic light coupling between III-V and beneath silicon. A thin SOI layer (typical thickness is 200-300 nm) as the

substrate is also desired for the purpose of dense photonic integration.

There have been a few integration configurations

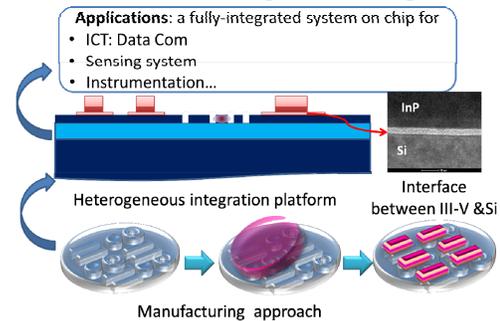


Fig.1 Heterogeneous III-V/Si integration as a platform technology.

demonstrated to date. Examples include hybrid III-V/Si evanescent waveguide structure, which is a SOI channel waveguide under the III-V epi-layers and the evanescent field is confined in the active region of III-V layers [1], adiabatic hybrid mode transformer structure based a pair of silicon and III-V waveguides and light confinement is controlled through the supermode of the pair waveguides[2], and III-V ridge waveguide on BCB (a polymer material) for light amplification and light is coupled down to silicon through an adiabatic coupler of which the III-V and silicon are contra-directional tapered [3]. These demonstrated configurations require an SOI channel waveguide under the III-V mesa (SOI is etched away for the case in Ref.[3]), a relatively thick SOI layer to match the III-V epi-layers or a long optical coupling structure (over 100 μm long) for light transfer between III-V and SOI layer.

II. HETEROGENEOUS III-V/SI PHOTONIC INTEGRATION CONFIGURATION AND OPTICAL COUPLING

The heterogeneous III-V/Si integration structure presented in this paper (see Fig.2) differs from the configurations mentioned above in: 1) III-V/Si active waveguide section and 2) adiabatic coupler for light transfer between the active waveguide section and SOI nanowaveguide. It also uses a thinner SOI layer as compared to the above examples [4-6].

The III-V epi-layers are directly bonded on SOI and etched till the n-contact layer to form a ridge III-V/Si waveguide as an active gain section. The SOI under the III-V is kept as a whole without channel waveguide, which provides a better thermal dissipation and flexibility in fabrication. Using a similar epi-layer structure in Ref.[1] and a 300 nm thick SOI as an example, the light confinement in the active region reaches its maximum

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(~20%) when the waveguide width is larger than 1.5 μm , which ensures the maximal modal gain for the heterogeneous III-V/Si photonic integration platform. The insets of Fig.2 illustrate the mode profile at different position.

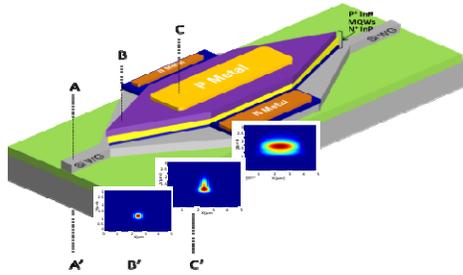


Fig.2 Heterogeneous III-V/Si integration structure and the corresponding mode profile at different position.

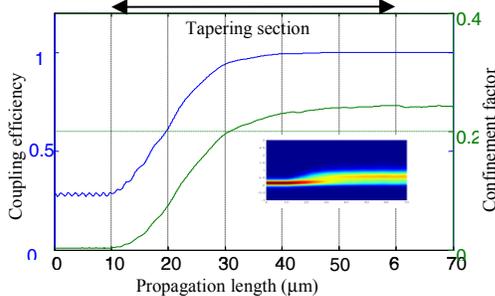


Fig.3 Simulation of adiabatic coupling efficiency.

The key features of the III-V/Si adiabatic coupler in Fig.1a are: 1) III-V and SOI are tapered in the SAME direction and SOI is always wider than III-V; 2) n-cladding layer in the tapering session is etched away. These features ensure an effective light coupling between III-V/Si ridge waveguide and thin SOI waveguide with a minimal reflection at the tapering end. In our experiment demonstration, we employed a tapering length of 50 μm (which is shorter than other configurations). The estimated light coupling efficiency and simulated field propagation of the structure is given in Fig.3, which shows the adiabatic coupling with efficiency close to 100%. An optimization of the tapering structure (using two-dimensional effective index method) can reduce the length to be as short as 25 μm while still retaining a coupling efficiency of ~100%[4].

The fabricated device is shown in Fig.4 (a-d), which is a 2mm long Fabry-Perot cavity laser consisting of silicon waveguide sections, two adiabatic coupler structures and a III-V/Si ridge waveguide section as the gain region. The III-V/Si laser can operate under continuous-wave (CW) at room-temperature [6] and the optical coupling between the III-V/Si section and SOI is about 90% verified by experiment [5]. The measured transmission spectrum using sub-bandgap wavelength (see Fig.4e-f) shows a response very close to that from a single FP cavity, which also suggests a reflection of about -37dB at the adiabatic tapering end.

The challenge in achieving efficient adiabatic coupling between III-V semiconductor layers and SOI layer by a compact structure is because of the thickness mismatch. The III-V epi-layers (p-i-n) bonded on silicon has a typical thickness of 2 μm , which is about 10 times thicker than the

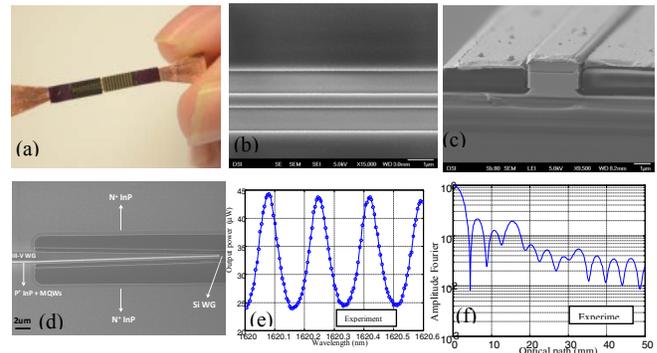


Fig.4 (a-d) fabricated laser device; (e-f) characterization of the FP spectrum response for coupling efficiency and tapering-end reflection.

SOI layer. To overcome this issue, the lateral current injection scheme can be employed. The thickness of III-V layers can be reduced significantly close to the SOI layer as the p-and n-cladding are placed in-plane in this lateral current injection scheme. The length of the adiabatic coupling can be therefore significantly shortened, which can be as short as only 4 μm according to our simulation and design, and also the light confinement in the active region can be improved due to the high-index contrast in the vertical direction. These features make it attractive to be the new-generation heterogeneous III-V/Si integration configuration.

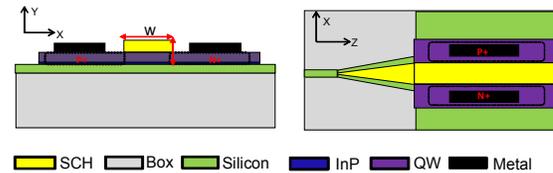


Fig.5 New generation heterogeneous III-V/Si integration based on lateral current injection.

III. CONCLUSION

The heterogeneous III-V/Si integration configuration as a platform technology has been presented. The efficient adiabatic optical coupling between the active III-V/Si ridge waveguide and thin SOI passive nanophotonic waveguide section is designed, demonstrated and analyzed.

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